



# SPEC CPU®2017 Integer Speed Result

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## Cisco Systems

Cisco UCS C220 M6 (Intel Xeon Platinum 8352V, 2.10GHz)

SPECspeed®2017\_int\_base = 11.7

SPECspeed®2017\_int\_peak = Not Run

CPU2017 License: 9019

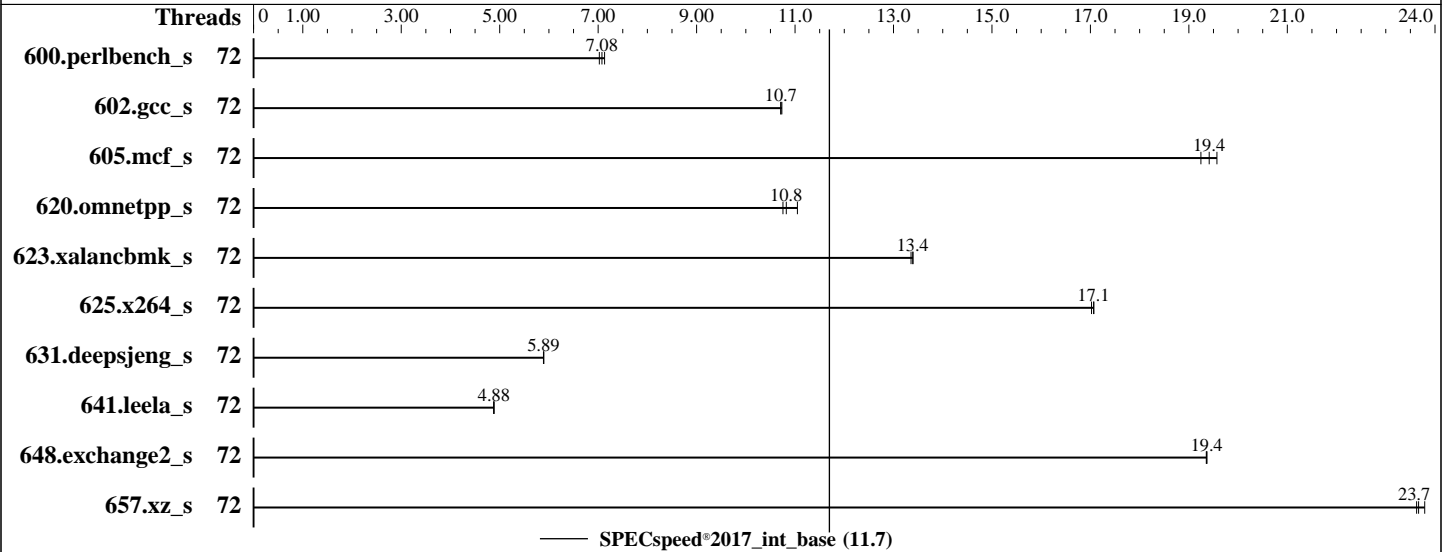
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Sep-2021

Hardware Availability: Apr-2021

Software Availability: Dec-2020



### Hardware

CPU Name: Intel Xeon Platinum 8352V  
 Max MHz: 3500  
 Nominal: 2100  
 Enabled: 72 cores, 2 chips  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 48 KB D on chip per core  
 L2: 1.25 MB I+D on chip per core  
 L3: 54 MB I+D on chip per chip  
 Other: None  
 Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2933)  
 Storage: 1 x 960 GB M.2 SSD SATA  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default  
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux  
 Parallel: Yes  
 Firmware: Version 4.2.1d released Jul-2021  
 File System: btrfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



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## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	72	253	7.02	249	7.13	<b><u>251</u></b>	<b><u>7.08</u></b>							
602.gcc_s	72	<b><u>372</u></b>	<b><u>10.7</u></b>	371	10.7	372	10.7							
605.mcf_s	72	<b><u>243</u></b>	<b><u>19.4</u></b>	241	19.6	245	19.2							
620.omnetpp_s	72	152	10.8	148	11.0	<b><u>151</u></b>	<b><u>10.8</u></b>							
623.xalancbmk_s	72	106	13.4	<b><u>106</u></b>	<b><u>13.4</u></b>	106	13.4							
625.x264_s	72	103	17.1	104	17.0	<b><u>103</u></b>	<b><u>17.1</u></b>							
631.deepsjeng_s	72	243	5.89	<b><u>243</u></b>	<b><u>5.89</u></b>	243	5.90							
641.leela_s	72	350	4.88	<b><u>349</u></b>	<b><u>4.88</u></b>	349	4.88							
648.exchange2_s	72	152	19.4	152	19.4	<b><u>152</u></b>	<b><u>19.4</u></b>							
657.xz_s	72	260	23.8	<b><u>261</u></b>	<b><u>23.7</u></b>	262	23.6							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"  
cpupower frequency-set -g performance run as root to set the scaling governor to performance.

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
KMP\_AFFINITY = "granularity=fine,scatter"  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
MALLOC\_CONF = "retain:true"  
OMP\_STACKSIZE = "192M"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM  
memory using Redhat Enterprise Linux 8.0  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

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### General Notes (Continued)

jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

### Platform Notes

BIOS Settings:

Intel Hyper-Threading Technology set to Disabled  
DCU Streamer Prefetch set to Disabled  
LLC Dead Line set to Disabled  
Memory Refresh Rate set to 1x Refresh  
ADDDC Sparing set to Disabled  
Patrol Scrub set to Disabled  
Energy Efficient Turbo set to Enabled  
Processor C6 Report set to Enabled  
Processor ClE set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d  
running on localhost Sat Sep 25 03:30:36 2021

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Platinum 8352V CPU @ 2.10GHz
 2 "physical id"s (chips)
 72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 36
siblings : 36
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31 32 33 34 35
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31 32 33 34 35
```

From lscpu from util-linux 2.33.1:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 1
```

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### Platform Notes (Continued)

```

Core(s) per socket: 36
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Platinum 8352V CPU @ 2.10GHz
Stepping: 6
CPU MHz: 800.488
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 55296K
NUMA node0 CPU(s): 0-35
NUMA node1 CPU(s): 36-71
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 55296 KB

```

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
28 29 30 31 32 33 34 35
node 0 size: 515574 MB
node 0 free: 514664 MB
node 1 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60
61 62 63 64 65 66 67 68 69 70 71
node 1 size: 515809 MB

```

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### Platform Notes (Continued)

```

node 1 free: 515410 MB
node distances:
node  0  1
  0:  10  20
  1:  20  10

From /proc/meminfo
MemTotal:      1056137236 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):          Not affected
CVE-2018-3620 (L1 Terminal Fault):      Not affected
Microarchitectural Data Sampling:      Not affected
CVE-2017-5754 (Meltdown):              Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store
Bypass disabled via prctl and
seccomp
CVE-2017-5753 (Spectre variant 1):      Mitigation: usercopy/swapgs
barriers and __user pointer
sanitization
CVE-2017-5715 (Spectre variant 2):      Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 25 03:29

```

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## Platform Notes (Continued)

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda2	btrfs	222G	33G	188G	15%	/home

From /sys/devices/virtual/dmi/id

```
Vendor:      Cisco Systems Inc
Product:    UCSC-C220-M6S
Serial:     WZP24430N7F
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2933

BIOS:

```
BIOS Vendor:    Cisco Systems, Inc.
BIOS Version:   C220M6.4.2.1d.0.0730210924
BIOS Date:      07/30/2021
BIOS Revision:  5.22
```

(End of data from sysinfo program)

## Compiler Version Notes

```
=====  
C      | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)  
      | 625.x264_s(base) 657.xz_s(base)  
-----
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
=====  
C++   | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)  
     | 641.leela_s(base)  
-----
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113  
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## Compiler Version Notes (Continued)

Fortran | 648.exchange2\_s(base)

-----  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

## Base Portability Flags

600.perlbench\_s: -DSPEC\_LP64 -DSPEC\_LINUX\_X64  
602 gcc\_s: -DSPEC\_LP64  
605.mcf\_s: -DSPEC\_LP64  
620.omnetpp\_s: -DSPEC\_LP64  
623.xalancbmk\_s: -DSPEC\_LP64 -DSPEC\_LINUX  
625.x264\_s: -DSPEC\_LP64  
631.deepsjeng\_s: -DSPEC\_LP64  
641.leela\_s: -DSPEC\_LP64  
648.exchange2\_s: -DSPEC\_LP64  
657.xz\_s: -DSPEC\_LP64

## Base Optimization Flags

C benchmarks:

-DSPEC\_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512  
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:

-DSPEC\_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math

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## Base Optimization Flags (Continued)

C++ benchmarks (continued):

```
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries  
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/  
-lqkmallocc
```

Fortran benchmarks:

```
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs -align array32byte -auto  
-mbranches-within-32B-boundaries
```

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.html](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html)

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revJ.html>

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.xml](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml)

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revJ.xml>

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