



SPEC[®] CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M4 (Intel Xeon E5-2699 v3 @ 2.30GHz)

SPECint[®]_rate2006 = Not Run

SPECint_rate_base2006 = 1380

CPU2006 license: 9019

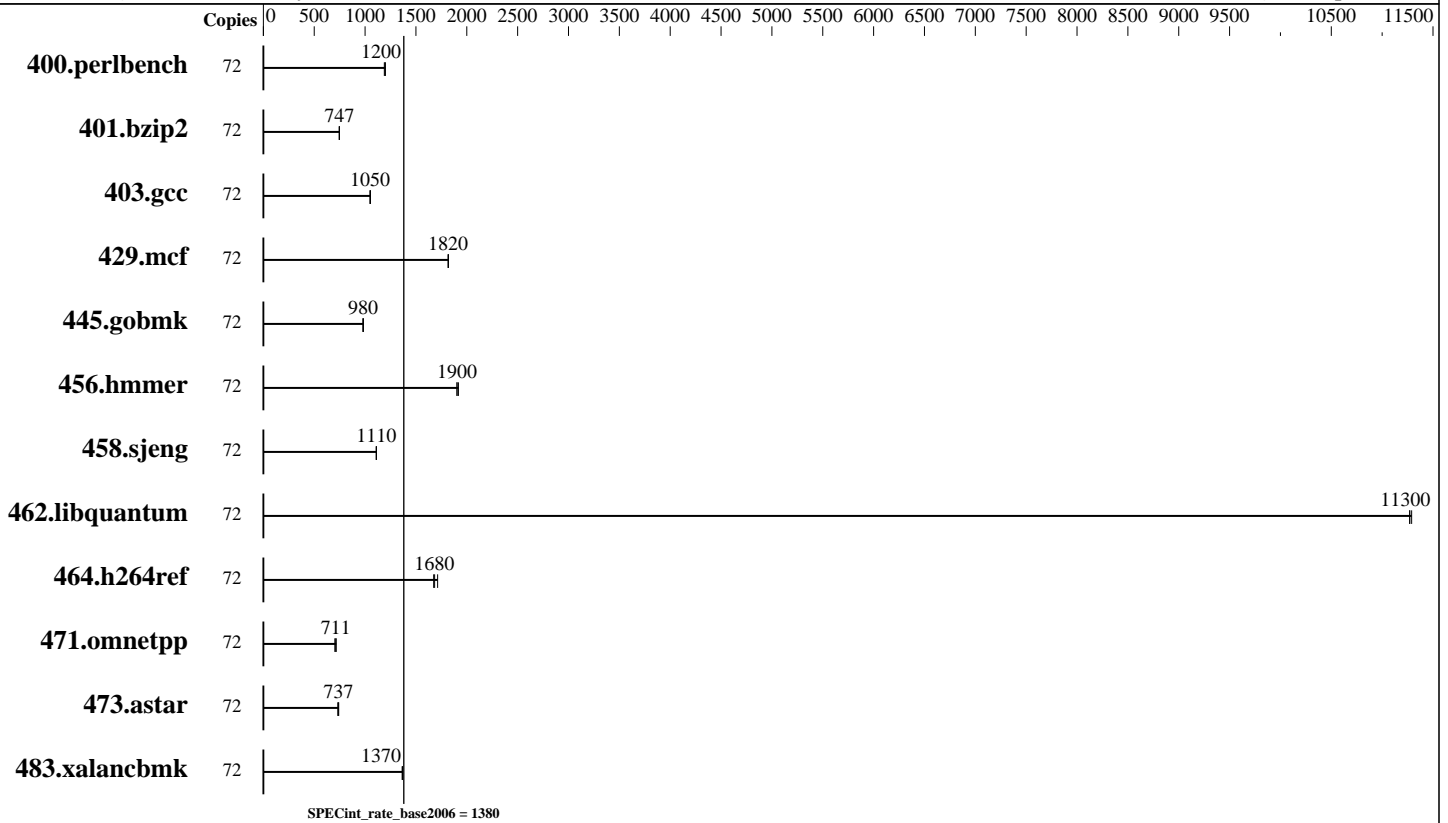
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Jun-2014

Hardware Availability: Sep-2014

Software Availability: Sep-2013



Hardware

CPU Name: Intel Xeon E5-2699 v3
 CPU Characteristics: Intel Turbo Boost Technology up to 3.60 GHz
 CPU MHz: 2300
 FPU: Integrated
 CPU(s) enabled: 36 cores, 2 chips, 18 cores/chip, 2 threads/core
 CPU(s) orderable: 1,2 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 256 KB I+D on chip per core
 L3 Cache: 45 MB I+D on chip per chip
 Other Cache: None
 Memory: 256 GB (16 x 16 GB 2Rx4 PC4-2133P-R)
 Disk Subsystem: 1 x 300GB SAS, 15K RPM
 Other Hardware: None

Software

Operating System: SUSE Linux Enterprise Server 11 (x86_64)
 3.0.76-0.11-default
 Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
 Auto Parallel: No
 File System: ext3
 System State: Run level 3 (multi-user)
 Base Pointers: 32-bit
 Peak Pointers: 32/64-bit
 Other Software: Microquill SmartHeap V10.0



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M4 (Intel Xeon E5-2699 v3 @ 2.30GHz)

SPECint_rate2006 = Not Run

SPECint_rate_base2006 = 1380

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jun-2014
Hardware Availability: Sep-2014
Software Availability: Sep-2013

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	72	586	1200	592	1190	588	1200							
401.bzip2	72	931	747	930	747	930	747							
403.gcc	72	550	1050	553	1050	552	1050							
429.mcf	72	361	1820	361	1820	361	1820							
445.gobmk	72	771	980	768	983	771	980							
456.hammer	72	353	1900	350	1920	353	1900							
458.sjeng	72	784	1110	784	1110	785	1110							
462.libquantum	72	132	11300	132	11300	132	11300							
464.h264ref	72	952	1670	946	1680	930	1710							
471.omnetpp	72	628	716	633	711	641	703							
473.astar	72	686	737	691	732	682	741							
483.xalancbmk	72	364	1370	364	1370	363	1370							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

```

CPU performance set to Enterprise
Power Technology set to Energy Efficient
Energy Performance BIAS setting set to Balanced Performance
Memory RAS configuration set to Maximum Performance
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on SLES11-CS Thu Jun 26 06:34:45 2014
This section contains SUT (System Under Test) info as seen by
some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo
From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2699 v3 @ 2.30GHz
2 "physical id"s (chips)
72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)

```

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M4 (Intel Xeon E5-2699 v3 @ 2.30GHz)

SPECint_rate2006 = Not Run

SPECint_rate_base2006 = 1380

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jun-2014
Hardware Availability: Sep-2014
Software Availability: Sep-2013

Platform Notes (Continued)

```

cpu cores : 18
siblings  : 36
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
cache size : 23040 KB
From /proc/meminfo
MemTotal:      264567896 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 11 (x86_64)
From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 11 (x86_64)
VERSION = 11
PATCHLEVEL = 3
uname -a:
Linux SLES11-CS 3.0.76-0.11-default #1 SMP Fri Jun 14 08:21:43 UTC 2013
(ccab990) x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Jun 26 06:28 last=S
SPEC is set to: /opt/cpu2006-1.2
Filesystem      Type Size Used Avail Use% Mounted on
/dev/sda2        ext3 273G  13G 259G   5% /
Additional information from dmidecode:
BIOS Cisco Systems, Inc. C220M4.2.0.3.0.080720142114 08/07/2014
Memory:
16x 0xCE00 M393A2G40DB0-CPB 16 GB 2133 MHz
8x NO DIMM NO DIMM
(End of data from sysinfo program)

```

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"
Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M4 (Intel Xeon E5-2699 v3 @ 2.30GHz)

SPECint_rate2006 = Not Run

SPECint_rate_base2006 = 1380

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jun-2014
Hardware Availability: Sep-2014
Software Availability: Sep-2013

Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.xml>



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M4 (Intel Xeon E5-2699 v3 @ 2.30GHz)

SPECint_rate2006 = Not Run

SPECint_rate_base2006 = 1380

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Jun-2014

Hardware Availability: Sep-2014

Software Availability: Sep-2013

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Thu Oct 30 12:50:41 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 30 October 2014.