SPEC CPU®2017 Floating Point Rate Result

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Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6238, 2.10GHz)

SPECrate®2017_fp_base = 444

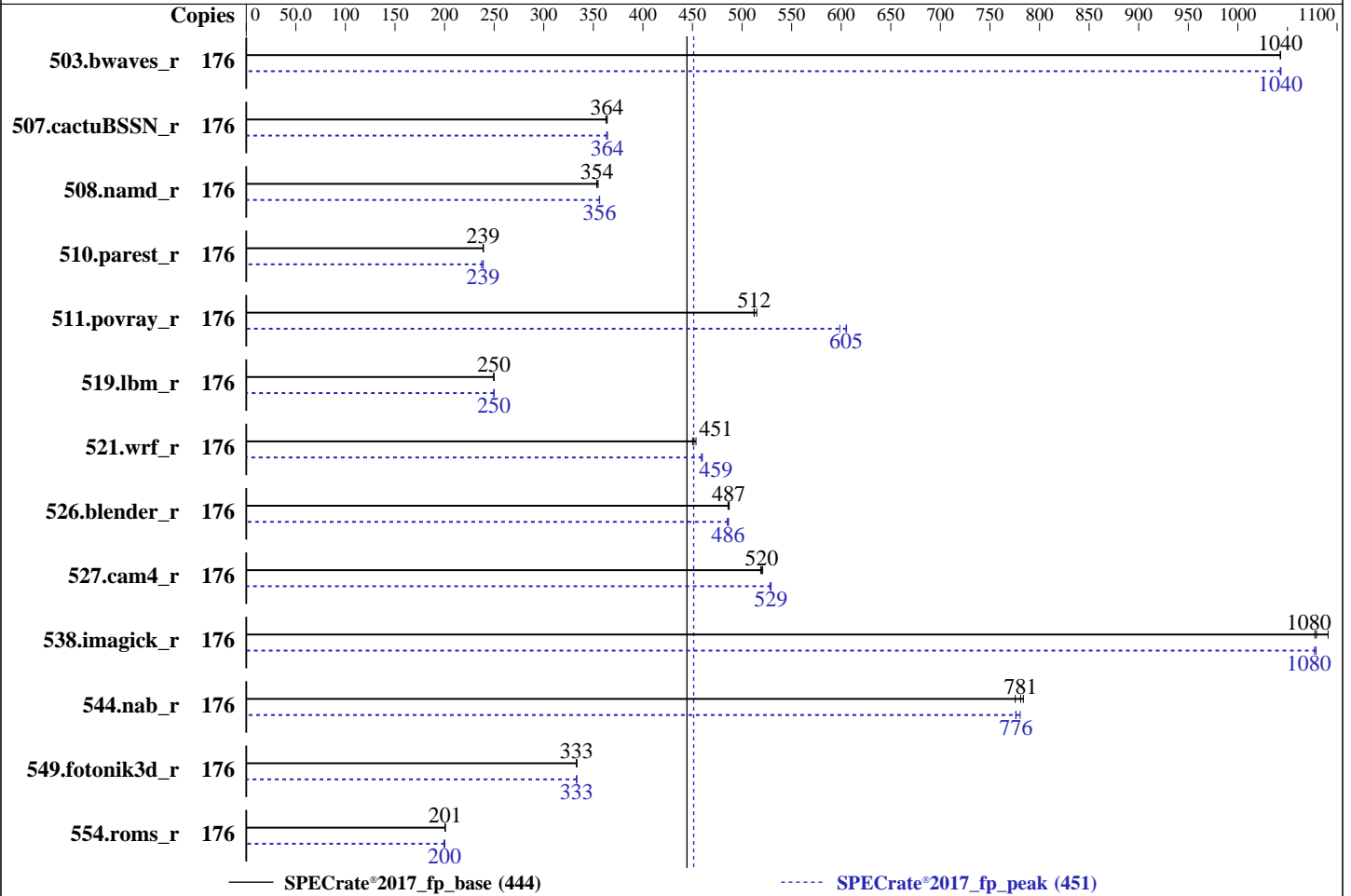SPECrate®2017_fp_peak = 451

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Copies		
503.bwaves_r	176	1040 / 1040
507.cactuBSSN_r	176	364 / 364
508.namd_r	176	354 / 356
510.parest_r	176	239 / 239
511.povray_r	176	512 / 605
519.lbm_r	176	250 / 250
521.wrf_r	176	451 / 459
526.blender_r	176	487 / 486
527.cam4_r	176	520 / 529
538.imagick_r	176	1080 / 1080
544.nab_r	176	781 / 776
549.fotonik3d_r	176	333 / 333
554.roms_r	176	201 / 200

SPECrate®2017_fp_base (444)
SPECrate®2017_fp_peak (451)

Hardware

CPU Name: Intel Xeon Gold 6238
 Max MHz: 3700
 Nominal: 2100
Enabled: 88 cores, 4 chips, 2 threads/core
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 30.25 MB I+D on chip per chip
 Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64)
4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++
Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran
Compiler for Linux
Parallel: No
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: BIOS set to prefer performance at the cost of additional power usage

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Results Table

Benchmark	Base						Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	176	**1692**	**1040**	1692	1040	1692	1040	176	1692	1040	**1692**	**1040**	1691	1040
507.cactuBSSN_r	176	612	364	**613**	**364**	614	363	176	612	364	**612**	**364**	613	363
508.namd_r	176	471	355	**472**	**354**	473	353	176	469	356	470	356	**469**	**356**
510.parest_r	176	1924	239	1928	239	**1928**	**239**	176	**1928**	**239**	1940	237	1926	239
511.povray_r	176	**802**	**512**	798	515	803	512	176	687	599	679	605	**679**	**605**
519.lbm_r	176	743	250	**743**	**250**	743	250	176	743	250	**743**	**250**	743	250
521.wrf_r	176	**873**	**451**	869	454	876	450	176	859	459	**858**	**459**	857	460
526.blender_r	176	550	487	552	486	**551**	**487**	176	**551**	**486**	553	485	551	486
527.cam4_r	176	593	519	**592**	**520**	591	521	176	582	529	583	528	**582**	**529**
538.imagick_r	176	406	1080	401	1090	**406**	**1080**	176	406	1080	**406**	**1080**	406	1080
544.nab_r	176	378	784	382	776	**379**	**781**	176	**382**	**776**	382	776	380	780
549.fotonik3d_r	176	**2058**	**333**	2060	333	2058	333	176	2060	333	2058	333	**2059**	**333**
554.roms_r	176	1393	201	**1394**	**201**	1396	200	176	**1398**	**200**	1403	199	1397	200

SPECrate®2017_fp_base =	**444**
SPECrate®2017_fp_peak =	**451**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches

(Continued on next page)

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General Notes (Continued)

```
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
```

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
 running on linux-icbf Sun Jan 12 09:11:53 2020

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6238 CPU @ 2.10GHz
       4  "physical id"s (chips)
       176 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 22
       siblings  : 44
       physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
       physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
       physical 2: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
       physical 3: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28

 From lscpu:
    Architecture:        x86_64
    CPU op-mode(s):      32-bit, 64-bit
    Byte Order:          Little Endian
    CPU(s):              176
    On-line CPU(s) list: 0-175
    Thread(s) per core:  2
    Core(s) per socket:  22
```

(Continued on next page)

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Platform Notes (Continued)

```
      Socket(s):            4
      NUMA node(s):         8
      Vendor ID:            GenuineIntel
      CPU family:           6
      Model:                85
      Model name:           Intel(R) Xeon(R) Gold 6238 CPU @ 2.10GHz
      Stepping:             7
      CPU MHz:              2100.000
      CPU max MHz:          3700.0000
      CPU min MHz:          1000.0000
      BogoMIPS:             4200.00
      Virtualization:       VT-x
      L1d cache:            32K
      L1i cache:            32K
      L2 cache:             1024K
      L3 cache:             30976K
      NUMA node0 CPU(s):    0-2,6-8,11-13,17,18,88-90,94-96,99-101,105,106
      NUMA node1 CPU(s):    3-5,9,10,14-16,19-21,91-93,97,98,102-104,107-109
      NUMA node2 CPU(s):    22-24,28-30,33-35,39,40,110-112,116-118,121-123,127,128
      NUMA node3 CPU(s):    25-27,31,32,36-38,41-43,113-115,119,120,124-126,129-131
      NUMA node4 CPU(s):    44-46,50-52,55-57,61,62,132-134,138-140,143-145,149,150
      NUMA node5 CPU(s):    47-49,53,54,58-60,63-65,135-137,141,142,146-148,151-153
      NUMA node6 CPU(s):    66-68,72-74,77-79,83,84,154-156,160-162,165-167,171,172
      NUMA node7 CPU(s):    69-71,75,76,80-82,85-87,157-159,163,164,168-170,173-175
      Flags:                fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
    aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
    sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
    tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
    epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
    vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
    avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
    xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
    ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
    ospke avx512_vnni arch_capabilities ssbd

 /proc/cpuinfo cache data
    cache size : 30976 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
    available: 8 nodes (0-7)
    node 0 cpus: 0 1 2 6 7 8 11 12 13 17 18 88 89 90 94 95 96 99 100 101 105 106
    node 0 size: 192095 MB
    node 0 free: 180027 MB
    node 1 cpus: 3 4 5 9 10 14 15 16 19 20 21 91 92 93 97 98 102 103 104 107 108 109
```

(Continued on next page)

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Platform Notes (Continued)

```
   node 1 size: 193526 MB
   node 1 free: 184524 MB
   node 2 cpus: 22 23 24 28 29 30 33 34 35 39 40 110 111 112 116 117 118 121 122 123 127
   128
   node 2 size: 193526 MB
   node 2 free: 184834 MB
   node 3 cpus: 25 26 27 31 32 36 37 38 41 42 43 113 114 115 119 120 124 125 126 129 130
   131
   node 3 size: 193526 MB
   node 3 free: 184794 MB
   node 4 cpus: 44 45 46 50 51 52 55 56 57 61 62 132 133 134 138 139 140 143 144 145 149
   150
   node 4 size: 193497 MB
   node 4 free: 184849 MB
   node 5 cpus: 47 48 49 53 54 58 59 60 63 64 65 135 136 137 141 142 146 147 148 151 152
   153
   node 5 size: 193526 MB
   node 5 free: 184896 MB
   node 6 cpus: 66 67 68 72 73 74 77 78 79 83 84 154 155 156 160 161 162 165 166 167 171
   172
   node 6 size: 193526 MB
   node 6 free: 184913 MB
   node 7 cpus: 69 70 71 75 76 80 81 82 85 86 87 157 158 159 163 164 168 169 170 173 174
   175
   node 7 size: 193523 MB
   node 7 free: 184900 MB
   node distances:
   node   0   1   2   3   4   5   6   7
     0:  10  11  21  21  21  21  21  21
     1:  11  10  21  21  21  21  21  21
     2:  21  21  10  11  21  21  21  21
     3:  21  21  11  10  21  21  21  21
     4:  21  21  21  21  10  11  21  21
     5:  21  21  21  21  11  10  21  21
     6:  21  21  21  21  21  21  10  11
     7:  21  21  21  21  21  21  11  10

 From /proc/meminfo
    MemTotal:       1583871460 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    os-release:
       NAME="SLES"
       VERSION="15"
       VERSION_ID="15"
```

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Platform Notes (Continued)

```
        PRETTY_NAME="SUSE Linux Enterprise Server 15"
        ID="sles"
        ID_LIKE="suse"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
   Linux linux-icbf 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault):        No status reported
Microarchitectural Data Sampling:         No status reported
CVE-2017-5754 (Meltdown):                 Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                          via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):        Mitigation: Indirect Branch Restricted
                                          Speculation, IBPB, IBRS_FW


run-level 3 Jan 9 16:42

SPEC is set to: /home/cpu2017
   Filesystem      Type   Size  Used Avail Use% Mounted on
   /dev/sdb2       btrfs  222G   76G  146G  35% /home

From /sys/devices/virtual/dmi/id
   BIOS:    Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
   Vendor:  Cisco Systems Inc
   Product: UCSB-B480-M5
   Serial:  FLM230102QU


Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory:
    48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C                  | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
```

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Compiler Version Notes (Continued)

```
                         | 544.nab_r(base, peak)
-------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
-------------------------------------------------------------------------------


===============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
-------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
-------------------------------------------------------------------------------


===============================================================================
C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)
-------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
-------------------------------------------------------------------------------


===============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
-------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
-------------------------------------------------------------------------------


===============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                | 554.roms_r(base, peak)
-------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
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```

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Compiler Version Notes (Continued)

```
--------------------------------------------------------------------------

==========================================================================
Fortran, C     | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
--------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

C++ benchmarks:
`icpc -m64`

Fortran benchmarks:
`ifort -m64`

Benchmarks using both Fortran and C:
`ifort -m64 icc -m64 -std=c11`

Benchmarks using both C and C++:
`icpc -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
`icpc -m64 icc -m64 -std=c11 ifort -m64`

Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`
507.cactuBSSN_r: `-DSPEC_LP64`
508.namd_r: `-DSPEC_LP64`
510.parest_r: `-DSPEC_LP64`
511.povray_r: `-DSPEC_LP64`
519.lbm_r: `-DSPEC_LP64`
521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`

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Base Portability Flags (Continued)

527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
538.imagick_r: `-DSPEC_LP64`
544.nab_r: `-DSPEC_LP64`
549.fotonik3d_r: `-DSPEC_LP64`
554.roms_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=4`

C++ benchmarks:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=4`

Fortran benchmarks:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=4 -auto`
`-nostandard-realloc-lhs -align array32byte`

Benchmarks using both Fortran and C:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=4 -auto`
`-nostandard-realloc-lhs -align array32byte`

Benchmarks using both C and C++:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=4`

Benchmarks using Fortran, C, and C++:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=4 -auto`
`-nostandard-realloc-lhs -align array32byte`

Peak Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

C++ benchmarks:
`icpc -m64`

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Peak Compiler Invocation (Continued)

Fortran benchmarks:
```
ifort -m64
```

Benchmarks using both Fortran and C:
```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Peak Optimization Flags

C benchmarks:

519.lbm_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

538.imagick_r: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

544.nab_r: `Same as 538.imagick_r`

C++ benchmarks:

508.namd_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

510.parest_r: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

Fortran benchmarks:

(Continued on next page)

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SPECrate®2017_fp_peak = 451

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

503.bwaves_r: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte`

549.fotonik3d_r: `Same as 503.bwaves_r`

554.roms_r: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte`

Benchmarks using both Fortran and C:
`-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte`

Benchmarks using both C and C++:

511.povray_r: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

526.blender_r: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

Benchmarks using Fortran, C, and C++:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html

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You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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