



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

CPU2017 License: 9019

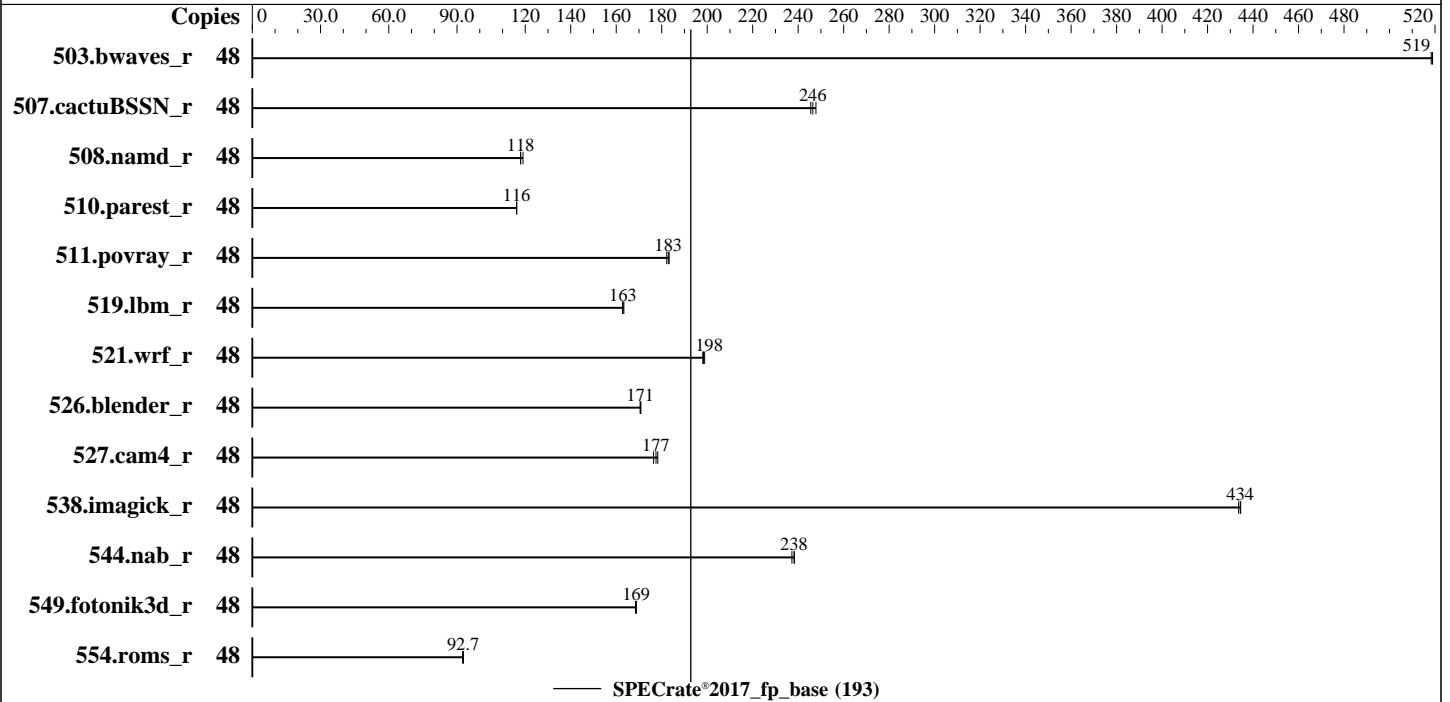
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2021

Hardware Availability: Jun-2021

Software Availability: Mar-2021



### Hardware

CPU Name: Intel Xeon Silver 4310  
 Max MHz: 3300  
 Nominal: 2100  
 Enabled: 24 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 48 KB D on chip per core  
 L2: 1.25 MB I+D on chip per core  
 L3: 18 MB I+D on chip per chip  
 Other: None  
 Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)  
 Storage: 2 x 240 GB SATA SSD  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default  
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux  
 Parallel: No  
 Firmware: Version 4.2.1c released Jul-2021  
 File System: btrfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Aug-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Mar-2021

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	48	<b>928</b>	<b>519</b>	928	519	929	518							
507.cactuBSSN_r	48	<b>247</b>	<b>246</b>	247	246	245	248							
508.namd_r	48	<b>386</b>	<b>118</b>	387	118	383	119							
510.parest_r	48	1081	116	<b>1080</b>	<b>116</b>	1080	116							
511.povray_r	48	<b>613</b>	<b>183</b>	615	182	612	183							
519.lbm_r	48	310	163	311	163	<b>310</b>	<b>163</b>							
521.wrf_r	48	541	199	<b>542</b>	<b>198</b>	543	198							
526.blender_r	48	428	171	<b>428</b>	<b>171</b>	429	171							
527.cam4_r	48	476	176	471	178	<b>473</b>	<b>177</b>							
538.imagick_r	48	<b>275</b>	<b>434</b>	275	435	275	434							
544.nab_r	48	<b>339</b>	<b>238</b>	339	238	340	237							
549.fotonik3d_r	48	1110	168	<b>1108</b>	<b>169</b>	1108	169							
554.roms_r	48	825	92.5	<b>823</b>	<b>92.7</b>	822	92.8							

SPECrate®2017\_fp\_base = **193**

SPECrate®2017\_fp\_peak = **Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
MALLOC\_CONF = "retain:true"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2021

**Hardware Availability:** Jun-2021

**Software Availability:** Mar-2021

### General Notes (Continued)

```
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

```
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

### Platform Notes

BIOS Settings:

```
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled
```

```
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Sat Aug 14 17:07:51 2021
```

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
 2 "physical id"s (chips)
48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings  : 24
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11
```

From lscpu from util-linux 2.33.1:

```
Architecture: x86_64
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2021

**Hardware Availability:** Jun-2021

**Software Availability:** Mar-2021

### Platform Notes (Continued)

```

CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
Address sizes:       46 bits physical, 57 bits virtual
CPU(s):              48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s):           2
NUMA node(s):       4
Vendor ID:           GenuineIntel
CPU family:          6
Model:               106
Model name:          Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
Stepping:            6
CPU MHz:             1340.114
CPU max MHz:         3300.0000
CPU min MHz:         800.0000
BogoMIPS:            4200.00
Virtualization:      VT-x
L1d cache:           48K
L1i cache:           32K
L2 cache:            1280K
L3 cache:            18432K
NUMA node0 CPU(s):  0-5,24-29
NUMA node1 CPU(s):  6-11,30-35
NUMA node2 CPU(s):  12-17,36-41
NUMA node3 CPU(s):  18-23,42-47
Flags:                fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 18432 KB

```

```

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Aug-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Mar-2021

### Platform Notes (Continued)

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 24 25 26 27 28 29
node 0 size: 515652 MB
node 0 free: 515339 MB
node 1 cpus: 6 7 8 9 10 11 30 31 32 33 34 35
node 1 size: 516092 MB
node 1 free: 515738 MB
node 2 cpus: 12 13 14 15 16 17 36 37 38 39 40 41
node 2 size: 516092 MB
node 2 free: 515827 MB
node 3 cpus: 18 19 20 21 22 23 42 43 44 45 46 47
node 3 size: 516089 MB
node 3 free: 515742 MB
node distances:
node  0  1  2  3
  0: 10 11 20 20
  1: 11 10 20 20
  2: 20 20 10 11
  3: 20 20 11 10

```

```

From /proc/meminfo
MemTotal:      2113460764 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

```

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

```

```

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

```

```

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

```

Kernel self-reported vulnerability status:

```

CVE-2018-12207 (iTLB Multihit):          Not affected
CVE-2018-3620 (L1 Terminal Fault):      Not affected

```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2021

Hardware Availability: Jun-2021

Software Availability: Mar-2021

### Platform Notes (Continued)

Microarchitectural Data Sampling:	Not affected
CVE-2017-5754 (Meltdown):	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling):	Not affected
CVE-2019-11135 (TSX Asynchronous Abort):	Not affected

run-level 3 Aug 14 17:06

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda2	btrfs	222G	14G	207G	7%	/home

```

From /sys/devices/virtual/dmi/id
Vendor:      Cisco Systems Inc
Product:     UCSC-C240-M6S
Serial:      WZP24460JDQ

```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory: 32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

```

BIOS:
  BIOS Vendor:      Cisco Systems, Inc.
  BIOS Version:     C240M6.4.2.1c.10.0723211453
  BIOS Date:        07/23/2021
  BIOS Revision:    5.22

```

(End of data from sysinfo program)

### Compiler Version Notes

```

=====
C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
=====

```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2021

**Hardware Availability:** Jun-2021

**Software Availability:** Mar-2021

### Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C++ | 508.namd\_r(base) 510.parest\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C++, C | 511.povray\_r(base) 526.blender\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C++, C, Fortran | 507.cactuBSSN\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
Fortran | 503.bwaves\_r(base) 549.fotonik3d\_r(base) 554.roms\_r(base)  
=====

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
Fortran, C | 521.wrf\_r(base) 527.cam4\_r(base)  
=====

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2021

**Hardware Availability:** Jun-2021

**Software Availability:** Mar-2021

## Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112\_000000  
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
 Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113  
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

-----

## Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icx

Benchmarks using both C and C++:

icpx icx

Benchmarks using Fortran, C, and C++:

icpx icx ifort

## Base Portability Flags

503.bwaves\_r: -DSPEC\_LP64  
 507.cactuBSSN\_r: -DSPEC\_LP64  
 508.namd\_r: -DSPEC\_LP64  
 510.parest\_r: -DSPEC\_LP64  
 511.povray\_r: -DSPEC\_LP64  
 519.lbm\_r: -DSPEC\_LP64  
 521.wrf\_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big\_endian  
 526.blender\_r: -DSPEC\_LP64 -DSPEC\_LINUX -funsigned-char  
 527.cam4\_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG  
 538.imagick\_r: -DSPEC\_LP64  
 544.nab\_r: -DSPEC\_LP64  
 549.fotonik3d\_r: -DSPEC\_LP64  
 554.roms\_r: -DSPEC\_LP64





# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2021

**Hardware Availability:** Jun-2021

**Software Availability:** Mar-2021

## Base Optimization Flags

### C benchmarks:

```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

### C++ benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

### Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

### Benchmarks using both Fortran and C:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
```

### Benchmarks using both C and C++:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

### Benchmarks using Fortran, C, and C++:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
```

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.html](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html)

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revG.html>



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECrate®2017\_fp\_base = 193

SPECrate®2017\_fp\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2021

**Hardware Availability:** Jun-2021

**Software Availability:** Mar-2021

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.xml](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml)

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revG.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-14 17:07:50-0400.

Report generated on 2021-09-01 14:18:57 by CPU2017 PDF formatter v6442.

Originally published on 2021-08-31.